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SUGHRUE MION ZINN MACPEAK & SEAS
2100 PENNSYLVANIA AVENUE NW
WASHINGTON, DC 200373202

EXAMINER	
DAY, HERNG DER	

ART UNIT	PAPER NUMBER
2123	14

DATE MAILED: 07/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/347,409	AKIMOTO ET AL.	
	Examiner	Art Unit	
	Herng-der Day	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-6 and 8-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-6 and 8-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This communication is in response to (1) Applicants' Reply (paper # 10) to Office Action dated December 19, 2002 (paper # 8), mailed April 1, 2003, and (2) Applicants' Reply (paper # 13) to Office Action dated April 7, 2003 (paper # 12), mailed April 21, 2003.

1-1. Claims 1 and 7 have been cancelled; claims 2-4 and 8-12 have been amended; claims 13 and 14 have been added; claims 2-6 and 8-14 are pending.

1-2. Claims 2-6 and 8-14 have been examined and claims 2-6 and 8-14 have been rejected.

Drawings

2. The corrected drawings were received on April 1, 2003. These drawings are acceptable.

Specification

3. The disclosure is objected to because of the following informalities:

Appropriate correction is required.

3-1. It appears that "the delay time degradation rate calculation 305" in line 12 of page 12 should be "the delay time degradation rate calculation 308".

4. The amendment filed April 1, 2003, is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material, which is not supported by the original disclosure, is as follows:

(1) Amended sentences at lines 2-4 of page 4 and lines 15-17 of page 6 in the original specification, as described in page 13 of paper # 10. Please refer to the corresponding rejections under 35 U.S.C. 112, first paragraph, as detailed in section **7** below.

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Objections

5. Claims 4 and 10 are objected to because of the following informalities. Appropriate correction is required.

5-1. Claim 4 recites the limitation "$T_{connected\_fresh}$" in the last third line of the claim. It is inconsistent with the limitation "$T_{connect\_fresh}$" used in the equation to calculate "$T_{connect\_aged}$".

5-2. Claim 10 recites the limitation "$T_{connected\_fresh}$" in the last third line of the claim. It is inconsistent with the limitation "$T_{connect\_fresh}$" used in the equation to calculate "$T_{connect\_aged}$".

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 3-6 and 9-12 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

For example, as described in lines 2-4 of page 4 and in lines 15-17 of page 6, the block-to-block delay time $T_{connect\_aged}$ is delay time of a signal passing between said two logic blocks connected to each other by a computer. However, it is unclear for one skilled in the art why two logic blocks are not connected to each other by only wire(s) or conductor(s) but by a computer. Accordingly, without undue experiment, it is unclear how one skilled in the art may make and/or use the invention by calculating the block-to-block aged signal delay time $T_{connect\_aged}$ of two logic blocks connected to each other by a computer because the calculation of the delay time introduced by the computer has not been disclosed in the specification.

Applicants argue, "The two cited sentences of the Specification contains the preposition "by" instead of "in". The Specification is amended" (page 13, paper # 10). This amendment introduces new matter because changes the preposition from "by the computer" to "in the computer" not only changes the scope but also has no support in the original specification, as detailed in section **4** above.

8. Claims 13 and 14 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As described from the last line of page 12 to line 4 of page 13, "the delay time calculation 402 is a conventional method for calculating delay time without reference to the hot electron effect". The new claim 13 recites the limitation "wherein in the first calculation means, the plurality of V_C values includes exclusively a V_C value of a transistor connected directly to an input pin of the logic block and a V_C value of a transistor connected directly to an output pin of

the logic block". However, the new subject matter "includes exclusively" does not appear to be supported in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 14 is rejected as being dependent on the rejected claim 13.

9. Claims 4, 6, 10, and 12 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As described in page 19, a logic block comprising three stage inverters each of which has the same delay time. When the input changes from low level to high level, λ is shown by expression (31) and when the input changes from high level to low level, λ is shown by expression (32). Based on expression (32), the delay time for input changes from high level to low level will be zero.

Also note, as defined in page 11, λ_{in} (λ_{out}) is the ratio of the delay time occurred at the input (output) pin to the delay time between the input pin and the output pin. Based on the above definition of λ, without undue experiment, it is unclear for one skilled in the art why the value of λ in expression (31) is not 1 / 2 because in the middle stage the input changes from high level to low level with zero delay time. Similarly, it is unclear for one skilled in the art about expressions (33) and (34) for four stage inverters.

Applicants argue the hot carrier damage (pages 13-14, paper # 10) without disclosing the relationship of delay time and hot carrier damage. However, λ is defined as the ratio of "delay time" instead of "hot carrier damage". Accordingly, Applicants' argument is unpersuasive.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 2-3, 5, 8-9, 11, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwanishi et al., U.S. Patent 6,047,247 issued April 4, 2000, and filed December 5, 1997, in view of Fang et al., U.S. Patent 6,278,964 issued August 21, 2001 and filed May 29, 1998.

11-1. Regarding claim 2, Iwanishi et al. disclose a method of calculating, by the use of a computer, a numerical value V_A representative of a circuit property of a logic level circuit, from a numerical value V_B, which shows a block property of a logic block included in the logic level circuit, the method comprising:

(a) calculating the value V_B (delays of the cells, delays of the cell-to-cell wirings, column 6, lines 39-40) from a plurality of numerical values V_C (circuit information of the LSI, column 6, line 37),

(b) calculating the value V_A from the value V_B, and outputting the value V_A as a value representative of a circuit property of said logic level circuit (delay calculation of an LSI, column 6, lines 35-36),

However, Iwanishi et al. do not expressly disclose: (1) each value V_C representing a transistor property of a transistor included in the logic block; and (2) the plurality of values V_C

comprises a first group of V_C values of transistors connected directly to an input pin of the logic block and a second group of V_C values of transistors connected directly to an output pin of the logic block. Nevertheless, Iwanishi et al. do suggest that the calculation of V_B based on circuit information (circuit information, column 6, lines 35-40).

Fang et al. disclose a detailed description of the IC cell data 102, which specifies characteristics and properties of the cells in the IC that are to be included in the simulation for hot-carrier effects (Fang, column 5, lines 38-45). IC cell data 102 includes the device model data to determine voltages and currents at each node within the cells. The device model data includes time-based mathematical models that typically include a set of device parameters and a set of complex equations which must be solved to simulate device performance (Fang, column 6, line 12 through column 7, line 39). In other words, Fang et al. disclose that the circuit information needed for simulating the hot-carrier effects includes a set of device (transistor) parameters (property of a transistor) for all devices including transistors connected directly to an input pin and transistors connected directly to an output pin.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Iwanishi et al. to incorporate the teachings of Fang et al. to obtain the invention as specified in claim 2 because Fang et al. disclose in detail the circuit information, which will be the input for simulating the hot-carrier effects, as suggested by Iwanishi et al.

11-2. Regarding claim 3, Iwanishi et al. disclose a method of calculating, by the use of a computer, a delay time of a signal passing through a logic level circuit which consists of a plurality of logic blocks from pin-to-pin delay time, which is delay time of a signal passing

between an input pin and an output pin of a logic block, and block-to-block delay time, which is delay time of a signal passing between two logic blocks connected to each other, comprising:

(a) calculating the pin-to-pin delay time and the block-to-block delay time without calculating in aging caused by hot carrier effect (delay calculation step, column 4, lines 53-63);

(b) calculating variations of signal delay times caused by aging (delay degradation amount calculation step, column 4, line 63 to column 5, line 9); and,

(c) modifying the pin-to-pin delay time and the block-to-block delay time calculated in step (a) by the variations calculated in step (b), and outputting said modified values for use as values representative of circuit properties of said logic level circuit (after-deterioration delay calculation step, column 5, lines 9-13).

However, Iwanishi et al. do not expressly disclose: (1) step (a) based on a value V_C of a transistor property of a transistor included in the logic block; and (2) step (b) based on the value V_C of a transistor connected to the input pin and the value V_C of a transistor connected to the output pin. Nevertheless, Iwanishi et al. disclose, "in FIG. 10, U1, U2, U3 are instances given to the cells" (column 7, lines 52-53), i.e., examples of a cell comprising a single inverter only. Iwanishi et al. also suggest that the delay calculation is conducted based on circuit information (circuit information, column 6, lines 35-40).

Fang et al. disclose a detailed description of the IC cell data 102, which specifies characteristics and properties of the cells in the IC that are to be included in the simulation for hot-carrier effects (Fang, column 5, lines 38-45). IC cell data 102 includes the device model data to determine voltages and currents at each node within the cells. The device model data includes time-based mathematical models that typically include a set of device parameters and a set of

complex equations which must be solved to simulate device performance (Fang, column 6, line 12 through column 7, line 39). In other words, Fang et al. disclose that the circuit information needed for simulating the hot-carrier effects includes a set of device (transistor) parameters (property of a transistor) for all devices including transistors connected to an input pin and transistors connected to an output pin.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Iwanishi et al. to incorporate the teachings of Fang et al. to obtain the invention as specified in claim 3 because Fang et al. disclose in detail the circuit information, which will be the input for simulating the hot-carrier effects, as suggested by Iwanishi et al.

11-3. Regarding claim 5, Iwanishi et al. further disclose a method of calculating, by the use of a computer, a delay time occurred to a signal passing through a logic level circuit that consists of a plurality of logic blocks, comprising:

(a) calculating delay times of all said logic blocks according to the method as in claim 3 (delay calculation step, delay degradation amount calculation step, and after-deterioration delay calculation step, column 4, line 53 to column 5, line 13; and analysis of section **11-2** above); and,

(b) calculating and outputting for use as a value representative of a circuit property of said logic level circuit the delay time of the logic level circuit from the result of step (a) (deterioration is estimated, column 5, lines 13-16).

11-4. Regarding claim 8, Iwanishi et al. disclose a computer-readable medium incorporating a program of instructions for calculating a numerical value V_A, which shows a property of a logic

level circuit, from a numerical value V_B, which shows a property of a logic block constituting the logic level circuit, the program making a computer execute the following processes:

(a) calculating the V_B value (delays of the cells, delays of the cell-to-cell wirings, column 6, lines 39-40) from a plurality of numerical values V_C (circuit information of the LSI, column 6, line 37),

(b) calculating the V_A value from the V_B value, and outputting the V_A value for use as a value representative of a circuit property of said logic level circuit (delay calculation of an LSI, column 6, lines 35-36).

However, Iwanishi et al. do not expressly disclose: (1) each V_C value showing a property of a transistor constituting part of the logic block; and (2) the plurality of V_C values comprises a V_C value of a transistor connected directly to an input pin of the logic block and another V_C value of a transistor connected directly to an output pin of the logic block. Nevertheless, Iwanishi et al. do suggest that the calculation of V_B based on circuit information (circuit information, column 6, lines 35-40).

Fang et al. disclose a detailed description of the IC cell data 102, which specifies characteristics and properties of the cells in the IC that are to be included in the simulation for hot-carrier effects (Fang, column 5, lines 38-45). IC cell data 102 includes the device model data to determine voltages and currents at each node within the cells. The device model data includes time-based mathematical models that typically include a set of device parameters and a set of complex equations which must be solved to simulate device performance (Fang, column 6, line 12 through column 7, line 39). In other words, Fang et al. disclose that the circuit information needed for simulating the hot-carrier effects includes a set of device (transistor) parameters

(property of a transistor) for all devices including transistors connected directly to an input pin and transistors connected directly to an output pin.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Iwanishi et al. to incorporate the teachings of Fang et al. to obtain the invention as specified in claim 8 because Fang et al. disclose in detail the circuit information, which will be the input for simulating the hot-carrier effects, as suggested by Iwanishi et al.

11-5. Regarding claim 9, Iwanishi et al. disclose a computer-readable medium incorporating a program of instructions for calculating a delay time of a signal passing through a logic level circuit which includes a plurality of logic blocks from pin-to-pin delay time, which is delay time of a signal passing between an input pin and an output pin of a logic block, and block-to-block delay time, which is delay time of a signal passing between two logic blocks connected to each other, the program making a computer execute the following processes:

(a) calculating the pin-to-pin delay time and the block-to-block delay time without calculating in aging caused by hot carrier effect (delay calculation step, column 4, lines 53-63);

(b) calculating variations of signal delay times caused by aging (delay degradation amount calculation step, column 4, line 63 to column 5, line 9); and,

(c) modifying the pin-to-pin delay time and the block-to-block delay time calculated in step (a) by the variations calculated in step (b), and outputting said modified values for use as values representative of circuit properties of said logic level circuit (after-deterioration delay calculation step, column 5, lines 9-13).

However, Iwanishi et al. do not expressly disclose step (b) based on values for the transistors connected directly to the input and output pins of logic block. Nevertheless, Iwanishi et al. disclose, "in FIG. 10, U1, U2, U3 are instances given to the cells" (column 7, lines 52-53), i.e., examples of a cell comprising a single inverter only. Iwanishi et al. also suggest that the delay calculation is conducted based on circuit information (circuit information, column 6, lines 35-40).

Fang et al. disclose a detailed description of the IC cell data 102, which specifies characteristics and properties of the cells in the IC that are to be included in the simulation for hot-carrier effects (Fang, column 5, lines 38-45). IC cell data 102 includes the device model data to determine voltages and currents at each node within the cells. The device model data includes time-based mathematical models that typically include a set of device parameters and a set of complex equations which must be solved to simulate device performance (Fang, column 6, line 12 through column 7, line 39). In other words, Fang et al. disclose that the circuit information needed for simulating the hot-carrier effects includes a set of device (transistor) parameters (property of a transistor) for all devices including transistors connected to an input pin and transistors connected to an output pin.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Iwanishi et al. to incorporate the teachings of Fang et al. to obtain the invention as specified in claim 9 because Fang et al. disclose in detail the circuit information, which will be the input for simulating the hot-carrier effects, as suggested by Iwanishi et al.

11-6. Regarding claim 11, Iwanishi et al. further disclose a computer-readable medium incorporating a program of instructions for calculating a delay time occurred to a signal passing through a logic level circuit that consists of a plurality of logic blocks, the program making a computer execute the following processes:

(a) calculating delay times of all said logic blocks according to the program as in claim 9 (delay calculation step, delay degradation amount calculation step, and after-deterioration delay calculation step, column 4, line 53 to column 5, line 13; and analysis of section **11-5** above); and,

(b) calculating and outputting for use as a value representative of a circuit property of said logic level circuit the delay time of the logic level circuit from the result of step (a) (deterioration is estimated, column 5, lines 13-16).

11-7. Regarding claim 13, Iwanishi et al. disclose a signal delay calculation system which calculates the delay time of a signal passing through a logic level circuit consisting of a plurality of logic blocks, the system comprising:

first calculation means for calculating value V_B, a property of a logic block constituting the logic level circuit (delays of the cells, column 6, lines 39-40), based on a plurality of numerical values V_C (circuit information of the LSI, column 6, line 37),

second calculation means for calculating a value V_A, representing a signal delay property of a logic level circuit, from values V_B (delay calculation of an LSI, column 6, lines 35-36); and

output means for outputting value V_A (deterioration is estimated, column 5, lines 13-16).

However, Iwanishi et al. do not expressly disclose: (1) the V_C value representing a property of a transistor included in the logic block; and (2) the plurality of values V_C includes a V_C value of a transistor connected directly to an input pin of the logic block and a V_C value of a

transistor connected directly to an output pin of the logic block. Nevertheless, Iwanishi et al. disclose, "in FIG. 10, U1, U2, U3 are instances given to the cells" (column 7, lines 52-53), i.e., examples of a cell comprising a single inverter only. Iwanishi et al. also suggest that the delay calculation is conducted based on circuit information (circuit information, column 6, lines 35-40).

Fang et al. disclose a detailed description of the IC cell data 102, which specifies characteristics and properties of the cells in the IC that are to be included in the simulation for hot-carrier effects (Fang, column 5, lines 38-45). IC cell data 102 includes the device model data to determine voltages and currents at each node within the cells. The device model data includes time-based mathematical models that typically include a set of device parameters and a set of complex equations which must be solved to simulate device performance (Fang, column 6, line 12 through column 7, line 39). In other words, Fang et al. disclose that the circuit information needed for simulating the hot-carrier effects includes a set of device (transistor) parameters (property of a transistor) for all devices including transistors connected to an input pin and transistors connected to an output pin.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Iwanishi et al. to incorporate the teachings of Fang et al. to obtain the invention as specified in claim 13 because Fang et al. disclose in detail the circuit information, which will be the input for simulating the hot-carrier effects, as suggested by Iwanishi et al.

11-8. Regarding claim 14, Iwanishi et al. further disclose V_A is an aging delay property of a logic level circuit (deterioration in reliability of the LSI, column 5, lines 13-16).

Allowable Subject Matter

12. The equations of claims 4, 6, 10, and 12 are deemed novel and non-obvious over the prior art of record, and would be allowable if the above rejections under 35 U.S.C. 112, first paragraphs are overcome.

Applicant's Arguments

13. Applicants argue the following:

(1) "Page 9-14 of the written disclosure as originally filed provides ample support for claims 3 and 5" (pages 11-12, paper # 10).

(2) "The two cited sentences of the Specification contains the preposition "by" instead of "in". The Specification is amended" (page 13, paper # 10).

(3) λ is based on whether the input or output stage inverter receives hot carrier damage (pages 13-14, paper # 10).

(4) "claims 7 and 9-11 are amended to use the language suggested by the Examiner" (pages 14-15, paper # 10).

(5) For 102(e) rejections, "Iwanishi does not disclose or suggest calculating signal delay times caused by aging based on values for the transistors connected directly to the input and output pins of logic blocks" (pages 15-16, paper # 10).

(6) For 103(a) rejections, "Feng does not disclose or suggest this calculation based on transistor values for transistors directly connected to the input pins and the output pins in a logic blocks" (pages 16-17, paper # 10).

(7) "One of the problems recognized and solved by Applicant's claimed invention is the need to calculate the hot-carrier effect faster and more simply by using fewer variables" (page 17, paper # 10).

(8) "New claims 13 and 14 are added. These claims contain no new matter" (page 17, paper # 10).

Response to Arguments

14. Applicants' arguments have been fully considered. They are unpersuasive except for arguments (1) and (4).

14-1. Response to Applicants' argument (1). In view of Applicants' persuasive argument, the original claim rejections under 35 U.S.C. 112, first paragraph (section **8**, paper # 8), have been withdrawn. However, as described from the last line of page 12 to line 4 of page 13 in the original specification, "the delay time calculation 402 is a conventional method for calculating delay time without reference to the hot electron effect", Applicants' argument implies calculating the delay time "based on a value V_C of a transistor property of a transistor included in the logic block" is a conventional method.

14-2. Response to Applicants' argument (2). In view of Applicants' unpersuasive argument, claims 3-6 and 9-12 are rejected under 35 U.S.C. 112, first paragraph, as detailed in section **7** above.

14-3. Response to Applicants' argument (3). In view of Applicants' unpersuasive argument, claims 4, 6, 10, and 12 are rejected under 35 U.S.C. 112, first paragraph, as detailed in section **9** above.

14-4. Response to Applicants' argument (4). The original claim rejections under 35 U.S.C. 112, second paragraph (section **11**, paper # 8), for indefiniteness have been withdrawn.

14-5. Response to Applicants' arguments (5)-(6). Iwanishi et al. disclose, "in FIG. 10, U1, U2, U3 are instances given to the cells" (column 7, lines 52-53), i.e., examples of a cell comprising a single inverter only. Therefore, it meets the limitation of "based on values for the transistors connected directly to the input and output pins of logic blocks", as detailed in sections **11-1** to **11-8** above.

14-6. Response to Applicants' argument (7). Only claims 4, 6, 10, and 12 are deemed novel and non-obvious over the prior art of record.

14-7. Response to Applicants' argument (8). In view of Applicants' unpersuasive argument, claims 13 and 14 are rejected under 35 U.S.C. 112, first paragraph, as detailed in section **8** above.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Reference to Huang et al., U.S. Patent 5,446,676 issued August 29, 1995, is cited as disclosing a transistor-level timing and power simulator and power analyzer.

Reference to Spyrou et al., U.S. Patent 5,841,672 issued November 24, 1998, and filed February 13, 1996, is cited as disclosing a method and apparatus for verifying signal timing of electrical circuits.

Reference to Yoshikawa et al., U.S. Patent 5,852,445 issued December 22, 1998, and filed November 2, 1995, is cited as disclosing a method of verifying integrated circuit operation.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Herng-der Day whose telephone number is (703) 305-5269. The examiner can normally be reached on 9:00 - 17:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J Teska can be reached on (703) 305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Herng-der Day
June 28, 2003

HUGH JONES PH.D.
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2100